

**REMARKS**

Claims 1-8 are pending in this application, and claim 1 is independent. No claims are amended or canceled. In light of the below remarks, favorable reconsideration and allowance of the present application are respectfully requested.

**Rejections Under 35 U.S.C. § 103 – JIN in view of YAMAGUCHI**

Claims 1-4 stand rejected under 35 U.S.C. §103(a) as being unpatentable over *Jin* in view of *Yamaguchi*. This rejection is respectfully traversed.

*Jin* allegedly teaches a silicon-on-insular dynamic threshold voltage MOSFET (SOI DTMOS) in FIG. 3. An Input 1 is said to be connected to stage n-1, which allegedly connects to an inverter containing a p-channel transistor and an n-channel transistor. An output 0 is allegedly connected to stage n, and FIG. 3 is said to further include a source Vdd and a source GND. (*Jin*, pages 1717-1718).

The Examiner correctly acknowledges that *Jin* cannot teach or suggest “a current source connected with the p-type base terminal of the n-channel MOS transistor” and “a current source connected with the n-type base terminal of the p-channel MOS transistor” and relies upon *Yamaguchi* in an attempt to cure this deficiency. (*Office Action*, page 3).

*Yamaguchi* allegedly teaches in FIG. 13 a bias selecting circuit 32' that is said to differ from the bias selecting circuit 32 in FIG. 8 by having an NMOS transistor 323 responsive to the control signal /CNT for selecting the substrate bias VBB3 and an NMOS transistor 324 responsive to the control signal CNT for selecting the substrate bias VBB4. All other features the bias selecting circuit 32' are said to be the same as the bias selecting circuit 32 shown in FIG. 8. (*Yamaguchi*, col. 12, lines 51-59).

*Yamaguchi* allegedly further teaches in FIG. 8 that the bias selecting circuit 32 includes NMOS transistors 321 and 322. The NMOS transistor 321 allegedly has its source connected to receive the substrate bias VBB1, its drain connected to the silicon substrate 1 together with the drain of the NMOS transistor 322, and its gate connected to receive the control signal/CNT. The NMOS transistor 322 is said to have its source connected to receive the substrate bias VBB2, and its gate connected to receive the signal CNT. *Yamaguchi* allegedly teaches that in operation, in the standby state, the control signal/CNT is set to the high level, NMOS transistor 321 is turned on, and the substrate bias VBB1 is supplied to the silicon substrate 1, and in the active state, the control signal CNT is set to the high level, the NMOS transistor 322 is turned on, and the substrate bias VBB2 is supplied to the silicon substrate 1. According to *Yamaguchi*, this structure allows the substrate bias applied to the silicon substrate 1 to be changed. (*Yamaguchi*, col. 11, lines 16-33). [Applicants refer the Examiner to FIG. 1, where *Yamaguchi* allegedly teaches that a semiconductor device 200, including a functional circuit 110, a first bias generating circuit 30, a second bias generating circuit 31, and a bias selecting circuit 32, is formed on a silicon substrate 1. (*Yamaguchi*, col. 8, lines 18-23).]

The Examiner alleges that NMOS transistor 321 connected to the NMOS of the inverter in FIG. 13 and NMOS transistor 323 connected with the PMOS of the inverter in FIG. 13 function as current sources. Applicants submit that, because the NMOS transistors 321 and 323 merely supply substrate bias VBB2 and VBB3 according to control signals CNT and /CNT, respectively, these transistors are used solely to bias the silicon substrate and cannot be considered current sources. In fact, *Yamaguchi* explicitly states in reference to FIG. 8 that “by this simple structure, the substrate bias applied to the silicon substrate 1 can be changed.” (*Yamaguchi*, col. 11, lines 32-33). Therefore, Applicants submit that nothing in *Yamaguchi*

teaches or suggests “a current source connected with the p-type base terminal of the n-channel MOS transistor” and “a current source connected with the n-type base terminal of the p-channel MOS transistor” as recited by claim 1.

Therefore, even if *Jin* and *Yamaguchi* could be combined (which Applicants do not admit or believe), nothing in *Yamaguchi* cures the deficiencies of *Jin* with respect to claim 1, and therefore Applicants respectfully request that this rejection of claim 1 be withdrawn. Applicants further request the rejections of claims 2-4 also be withdrawn, at least by virtue of their dependency upon claim 1.

**Rejections Under 35 U.S.C. § 103 – JIN in view of YAMAGUCHI, SHIMOMURA et al.**

Claims 5-8 stand rejected under 35 U.S.C. §103(a) as being unpatentable over *Jin* in view of *Yamaguchi*, and in further view of *Shimomura et al.* (as cited in the Information Disclosure Statement dated September 29, 2005). This rejection is respectfully traversed.

Applicants submit that, even if *Shimomura* could be combined with *Jin* and *Yamaguchi* (which Applicants do not admit or believe), nothing in *Shimomura* cures the deficiencies of *Jin* and *Yamaguchi* discussed above with respect to claim 1. Therefore, Applicants respectfully request that this rejection of claims 5-8 be withdrawn, at least by virtue of their dependency upon claim 1.

**CONCLUSION**

In view of the above remarks and amendments, Applicants respectfully submit that each of the rejections has been addressed and overcome, placing the present application in condition for allowance. A notice to that effect is respectfully requested. If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to contact the undersigned.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Donald J. Daley, Reg. No. 34,313 at the telephone number of the undersigned below.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,  
HARNESS, DICKY, & PIERCE, P.L.C.

By



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